

Amendments to the Claims

1. (Canceled)

2. (Canceled)

3. (Canceled)

4. (Canceled)

5. (Canceled)

6. (Canceled)

7. (Canceled)

8. (Canceled)

9. (Canceled)

10. (Canceled)

11. (Canceled)

12. (Canceled)

13. (Canceled)

14. (Canceled)

15. (Canceled)

16. (Canceled)

17. (Canceled)

18. (Canceled)

19. (Canceled)

20. (Canceled)

21. (Canceled)

22. (Canceled)

23. (Canceled)

24. (Canceled)

25. (Canceled)

26. (Canceled)

27. (Canceled)

28. (Canceled)

29. (Canceled)

30. (Canceled)

31. (Canceled)

32. (Canceled)

33. (Canceled)

34. (Currently Amended) A phase locked loop, comprising:

reference oscillator means for generating a low phase noise reference frequency
signal;

a voltage controlled oscillator for producing a desired output frequency signal;

a phase detector for comparing a phase of the low phase noise reference frequency signal to the desired output frequency signal; and

a loop filter for suppressing components of the low phase noise reference frequency signal;

wherein the reference oscillator means has a differential crystal oscillator circuit with a resonating crystal across differential outputs.

35. (Canceled)

36. (Canceled)

37. (Canceled)

38. (Canceled)

39. (Canceled)

40. (Canceled)

41. (Canceled)

42. (New) The phase locked loop of claim 34, wherein the reference oscillator means further comprises:

a first capacitor coupled to a first output terminal of the differential outputs;

a second capacitor coupled to a second output terminal of the differential outputs;

and

a differential oscillator driver circuit coupled to the first output terminal and the second output terminal.

43. (New) The phase locked loop of claim 42, wherein the first capacitor is further coupled to a ground and the second capacitor is further coupled to the ground.

44. (New) The phase locked loop of claim 34, wherein the reference oscillator means is configured to maintain a substantially pure differential sinusoidal signal across the differential outputs.

45. (New) The phase locked loop of claim 34, wherein the reference oscillator means further includes a linear buffer amplifier.

46. (New) The phase locked loop of claim 45, wherein the linear buffer amplifier is configured to receive a differential signal from the resonating crystal.

47. (New) The phase locked loop of claim 46, wherein the linear buffer amplifier is further configured to reduce a phase noise from the differential signal.

48. (New) The phase locked loop of claim 45, wherein the reference oscillator means further includes a nonlinear amplifier.

49. (New) The phase locked loop of claim 48, wherein the nonlinear amplifier is configured to receive a differential signal from the linear buffer amplifier.

50. (New) The phase locked loop of claim 49, wherein the nonlinear amplifier is further configured to reduce a phase noise from the differential signal.

51. (New) The phase locked loop of claim 34, wherein the reference oscillator means is configured to control a frequency of the desired output frequency signal.

52. (New) The phase locked loop of claim 51, wherein the frequency is equal to a reference frequency of the low phase noise reference frequency signal.

53. (New) The phase locked loop of claim 51, wherein the frequency is equal to a multiple of a reference frequency of the low phase noise reference frequency signal.

54. (New) The phase locked loop of claim 34, wherein the reference oscillator means is configured to control a phase of the desired output frequency signal.

55. (New) A phase locked loop, comprising:
a reference oscillator configured to produce a differential low phase noise signal having a reference frequency;
a phase detector coupled to the reference oscillator;
a loop filter coupled to the phase detector; and
a voltage controlled oscillator coupled to the loop filter and configured to produce a signal having a desired frequency;
wherein the reference oscillator has a differential crystal oscillator circuit with a resonating crystal across differential outputs.

56. (New) The phase locked loop of claim 55, wherein the desired frequency is equal to the reference frequency.

57. (New) The phase locked loop of claim 55, wherein the desired frequency is equal to a multiple of the reference frequency.

58. (New) A phase locked loop, comprising:

a reference oscillator configured to produce a differential low phase noise signal

having a reference frequency;

a voltage controlled oscillator configured to produce a signal having a desired frequency;

a phase detector coupled between the reference oscillator and the voltage controlled oscillator; and

a loop filter coupled between the reference oscillator and the voltage controlled oscillator;

wherein the reference oscillator has a differential crystal oscillator circuit with a resonating crystal across differential outputs.

59. (New) The phase locked loop of claim 58, wherein the desired frequency is equal to the reference frequency.

60. (New) The phase locked loop of claim 58, wherein the desired frequency is equal to a multiple of the reference frequency.

This listing of claims will replace all prior versions, and listings of claims in the application.